REMARKS

In response to the Office Action mailed September 1, 2005, Applicant respectfully requests reconsideration. To further the prosecution of this Application, Applicant has amended claims and submits the following remarks. The claims as now presented are believed to be in allowable condition.

Claims 34, 35 and 37 have been amended. Claims 2-7, 9-14, 16-21 and 23-37 are now pending in this Application. Claims 34-37 are independent claims.

Claim Objections/Rejections under §112

Claims 34, 35 and 37 have been amended to address the objections in paragraphs 3-4 and 6 of the Office Action.

Rejections under §102 and §103

Claims 2, 4-7, 9, 11-14, 16, 18-21 and 34-37 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,680,637 of Hotta et al. (Hotta), and claims 23-33 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hotta. Claims 3, 10 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hotta in view of U.S. Patent No. 5,748,978 of Narayan et al. (Narayan). Applicant respectfully traverses each of these rejections and requests reconsideration. The claims are in allowable condition.

Regarding the rejection of claims under 35 U.S.C. § 102:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Also, "the identical invention must be shown in as complete detail as is contained in the ... claim."
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> *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Also, in order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), the Office Action must meet three criteria.

> "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added)

It is respectfully submitted that Hotta, either by itself or in combination with Narayan, fails to show all the elements of the claims, and that therefore the claims are allowable in view of the teaching of these references.

Claim 34 includes the following elements (emphasis added):

...a memory circuit board that includes a shared data structure utilized in managing the use of a cache that temporarily stores copies of data elements stored in a set of storage devices;

... a processor circuit board that operates as at least one of a front-end interface between an external device and the cache and a back-end interface between the cache and the set of storage devices, the processor circuit board being operative with the memory circuit board to perform memory operations including ... (2) a complex operation to manipulate the shared data structure;

wherein the memory circuit board performs its part of the memory operations by:

(i) receiving from the processor circuit board a communication that includes a command field and a payload field;

(ii) determining whether the command field contains a basic write command or a script command, the basic write command

being present when the communication is generated by the processor circuit board as part of the basic operation, the script command being present when the communication is generated as part of the complex operation;

(iii) if the command field of the communication contains the basic write command, then writing data from the payload field of the communication into the memory location; and

(iv) if the command field of the communication contains the script command, then performing the following steps:

parsing the payload of the communication to identify a series of individual instructions; and

performing a series of operations on the shared data structure according to the series of individual instructions.

Hotta shows a RISC processor arranged to reduce a code size, make the hardware less complicated, execute a plurality of operations for one machine cycle, and enhance the performance. The processor is capable of executing N instruction each having a short word length for indicating a single operation or an instruction having a long word length for indicating M (N<M) operations. When the number of operations to be executed in parallel is large, the long-word instruction is used. When it is small, the short-word instruction is used. A competition between the long-word instructions is detected by hardware and a competition between the short-word instructions only is detected by software. The simplification of the hardware brings about improvement of a machine cycle, improvement of a code cache hit ratio caused by the reduction of a code size and increase of the number of operations to be executed in parallel for the purpose of enhancing the performance.

Thus, Hotta is not at all concerned with data storage devices such as disk drives, nor with any mechanisms for operating on shared data structures that are used in managing a cache that temporarily stores copies of data elements stored

in a set of storage devices. Hotta's teaching is limited to the internal structure and operation of a general-purpose RISC processor.

More specifically, Hotta is not seen to teach the portions of claim 34 identified by underlining above. Contrary to the assertion in the Office Action, Hotta is not seen to show a shared data structure that is used in managing a cache. The Office Action attempts to equate the claimed shared data structure with the entire memory 1200 of Hotta, but this is clearly not correct. A data structure is an organization of data that is understood by application software, such as an LRU queue or a hash list which are examples set forth in the present application (see page 18, e.g.). Hotta's memory is simply a container for data, not a data structure. No specific data or data structure is described in Hotta. Nor is there any description in Hotta of any management of a cache via the memory. Thus Hotta's memory is not the same as the claimed shared data structure.

Hotta's processor, which is shown in Figures 1 and 13 for example, is nowhere described as either a front-end interface between an external device and a cache or as a back-end interface between the cache and a set of storage devices. As already noted, Hotta does not discuss storage devices at all. Although the Office Action attempts to equate the claimed storage devices with the processor general purpose registers shown in Figure 2 of Hotta, this characterization is incorrect. It should be clear that in claim 34 the processor and storage devices are separate things. However, Hotta's general purpose registers are a core part of the processor itself. Hotta's processor cannot accurately be characterized as an interface to its own general purpose registers. Nor does Hotta discuss any interface function performed by the processor with respect to either of the processor caches (I cache 1300 or D cache 1306), and again any such characterization would not make sense. Both of these caches are also part of the processor, insofar as they store data and instructions that are provided to the instruction control unit 1303 and integer operating unit 1304, for example. Those units are not simply "interfaces" between the respective cache and some

external device; they are part of an overall self-contained finite state machine (which includes the I and D caches) that is referred to as a "processor".

Moreover, Hotta's processor is not seen to perform a complex operation to manipulate a shared data structure as set forth in claim 1. Given that no such shared data structure is shown in Hotta, clearly there can be no description of any type of operation thereon.

Finally, Hotta is not seen to show a memory circuit board that performs any of the functional steps (i) - (iv) of claim 1. Hotta's basic and compound instructions are performed by the processor itself, not by the memory. The memory plays the typical role of a processor memory in Hotta, namely to respond to hardware-level address and control signals generated as part of read and write (load/store) operations, which operations are performed by the processor as part of executing instructions that it has decoded. Thus the memory in Hotta does not perform any of the functions (i) - (iv) recited in claim 34.

Indeed, even the processor of Hotta does not perform the functionality recited in claim 34. If the instruction MSB is taken as the command field as alleged in the Office Action, then this field never contains a basic write command or a script command. The MSB is only an indicator that either a basic command or a compound command is present elsewhere in the instruction - it is never a basic command (such as a store command) itself. Additionally, if the remainder of the instruction is taken as the payload as alleged in the Office Action, then there is no case in which the contents of this field are written to a memory location. For the basic store instruction in Hotta, the contents of the instruction include an operation code, a size, and three register numbers S1, S2 and T as shown in Figure 3 of Hotta. These values are not written to a memory location, but rather used to identify which general-purpose registers contain the memory address and data. Thus Hotta does not show functions (ii) or (iii) of claim 34.

In summary, Hotta fails to show several elements of claim 34 as described above, and therefore claim 34 cannot be anticipated by Hotta under 35 U.S.C. §

102(b). Accordingly, claim 34 is seen to be allowable notwithstanding the teaching of Hotta and the other art of record.

The remaining claims incorporate, either directly or indirectly, features such as those discussed above with respect to claim 34. As these features are missing from Hotta, and have not alleged to be shown in Narayan (and indeed are not seen to be shown in Narayan either), the remaining claims are also seen to be allowable under both 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) in view of Hotta by itself or taken in combination with Narayan.

Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Response, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicant's Representative at the number below. An Applicant Initiated Interview Request Form is enclosed herewith for this purpose - to discuss any issues that may be remaining after consideration of this amendment.

Applicant hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-3661.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 616-2900, in Westborough, Massachusetts.

Respectfully submitted,

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